CLAIMS

What is claimed is:

1.   A method for characterizing an electronic circuit comprising:

    receiving design information from a circuit design tool;

5   identifying an electrical circuit condition that requires test based on the design
information;

    determining a design verification test;

    evaluating the effectiveness of the design verification test in exercising the electrical
circuit condition; and

10   determining a second design verification test and also evaluating the effectiveness of the
second design verification test in exercising the electrical circuit condition when the
first design verification test does not effectively exercise the electrical circuit
condition.

2.   The method of Claim 1 wherein determining a design verification test comprises:

15   generating a design verification test using one or more of a manual test definition
process, an algorithmic test definition process, a random test definition process and an
exhaustive test definition process.

3.   The method of Claim 1 wherein evaluating the effectiveness of the design verification test
comprises:

20   executing the design verification test in a simulator; and

    recognizing the presence of the electrical circuit condition in the simulator results.

4.   The method of Claim 1 wherein evaluating the effectiveness of the design verification test
comprises:

    representing the electrical condition in a simulator monitor function;

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executing the design verification test and the simulator monitor function in a simulator; and

monitoring the activity of the simulator monitor function.

5. The method of Claim 1 wherein receiving design information comprises:

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    parsing an output report from a circuit design tool; and

    generating tokens representing the parsed output report.

6. The method of Claim 1 wherein identifying an electrical circuit condition comprises one or more of identifying a noise event, identifying a coupling event, identifying a timing event, identifying a race event and identifying a dynamic hazard.

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7. The method of Claim 1 wherein identifying an electrical circuit condition comprises:

    receiving tokens descriptive of the design information; and

    analyze the structure of the tokens in accordance with a pre-established electrical event definition.

8. The method of Claim 1 wherein evaluating the effectiveness of the design verification test

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    comprises:

    generating a description file readable by one or more of an automatic test pattern generator, a fault simulator, and a vector tester; and

    causing one or more of an automatic test pattern generator, a fault simulator, and a vector tester to be executed using said generated description file as an input.

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9. The method of Claim 1 further comprising:

    receiving the electrical circuit condition in a design verification tool; and

    verifying the design of the electronic circuit based on the electrical circuit condition.

10. The method of Claim 9 wherein verifying the design comprises simulating one or more of a noise event, a coupling event, a timing event, a race event, and a dynamic hazard.

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11. The method of Claim 9 wherein verifying the design comprises automatically generating a test pattern for testing one or more of a noise event, a coupling event, a timing event, a race event, and a dynamic hazard.

12. An apparatus for characterizing an electronic circuit comprising:

5   design information receiver capable of receiving design information;

circuit condition identifier capable of identifying an electrical circuit condition in the design information that requires test;

design verification test selection unit capable of selecting a first design verification test; and

10   evaluation unit capable of evaluating the effectiveness of the first selected design verification test in exercising the identified circuit condition and wherein the design verification test selection unit is capable of selecting a second design verification test when the evaluation unit determines that the first selected design verification test is ineffective in exercising the identified circuit condition and wherein the evaluation

15   unit is capable of evaluating the effectiveness of the second selected design verification test.

13. The apparatus of Claim 12 wherein the design verification test selection unit comprises one or more of a manual test definition module, an automated test definition module, a random test definition module, and an exhaustive test definition module.

20 14. The apparatus of Claim 12 wherein the evaluation unit comprises:

executive module that conveys the design verification test to a simulator; and

analyzer module that receives results from the simulator and issues a signal when the electrical circuit condition is recognized in said simulator results.

15. The apparatus of Claim 12 wherein the evaluation unit comprises:

25   simulator monitor function receiver capable of receiving a simulator monitor function;

executive module that conveys the design verification test and the received simulator monitor function to a simulator; and

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analyzer module that issues a signal when the simulator monitor function is triggered.

16. The apparatus of Claim 12 wherein the design information receiver comprises a lexical analyzer capable of generating tokens according to an output report received from a circuit design tool.

5   17. The apparatus of Claim 12 wherein the circuit condition identifier comprises a parser capable of identifying one or more of a noise event, a coupling event, a timing event, a race event and a dynamic hazard.

18. The apparatus of Claim 12 wherein the circuit condition identifier comprises a parser capable of analyzing the structure of received tokens in accordance with a pre-established electrical
10   event definition.

19. The apparatus of Claim 12 wherein the evaluation unit comprises:
        description file generator capable of generating a description file that is readable by one
            or more of an automatic test pattern generator, a fault simulator, and a vector tester;
            and
15   test executive module capable of starting one or more of an automatic test pattern
            generator, a fault simulator, and a vector tester using said generated description file as
            an input.

20. The apparatus of Claim 12 further comprising a design verification director capable of:
        directing the received electrical condition to a design verification tool;
20   starting a design verification tool;
        receiving an output from the design verification tool; and
        issuing a signal when the identified electrical circuit condition is not detected in the
            received design verification tool output.

21. A computer-readable medium having computer-executable functions for characterizing an
25   electronic circuit comprising:

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receiving design information from a circuit design tool;

identifying an electrical circuit condition that requires test based on the design information;

determining a design verification test;

5   evaluating the effectiveness of the design verification test in exercising the electrical circuit condition; and

determining a second design verification test and also evaluating the effectiveness of the second design verification test in exercising the electrical circuit condition when the first design verification test does not effectively exercise the electrical circuit

10   condition.

22. The computer-readable medium of Claim 21 wherein determining a design verification test comprises:

generating a design verification test using one or more of a manual test definition process, an algorithmic test definition process, a random test definition process and an

15   exhaustive test definition process.

23. The computer-readable medium of Claim 21 wherein evaluating the effectiveness of the design verification test comprises:

executing the design verification test in a simulator; and

recognizing the presence of the electrical circuit condition in the simulator results.

20   24. The computer-readable medium of Claim 21 wherein evaluating the effectiveness of the design verification test comprises:

representing the electrical condition in a simulator monitor function,

executing the design verification test and the simulator monitor function in a simulator; and

25   monitoring the activity of the simulator monitor function.

25. The computer-readable medium of Claim 21 wherein receiving design information comprises:

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parsing an output report from a circuit design tool; and

generating tokens representing the parsed output report.

26. The computer-readable medium of Claim 21 wherein identifying an electrical circuit condition comprises one or more of identifying a noise event, identifying a coupling event,

5   identifying a timing event, identifying a race event, and identifying a dynamic hazard.

27. The computer-readable medium of Claim 21 wherein identifying an electrical circuit condition comprises:

receiving tokens descriptive of the design information; and

analyze the structure of the tokens in accordance with a pre-established electrical event

10   definition.

28. The computer-readable medium of Claim 21 wherein evaluating the effectiveness of the design verification test comprises:

generating a description file readable by one or more of an automatic test pattern generator, a fault simulator, and a vector tester; and

15   causing one or more of an automatic test pattern generator, a fault simulator, and a vector tester to be executed using said generated description file as an input.

29. The computer-readable medium of Claim 21 further comprising:

receiving the electrical circuit condition in a design verification tool; and

verifying the design of the electronic circuit based on the electrical circuit condition.

20 30. The computer-readable medium of Claim 29 wherein verifying the design comprises simulating one or more of a noise event, a coupling event, a timing event, a race event, and a dynamic hazard.

31. The computer-readable medium of Claim 29 wherein verifying the design comprises automatically generating a test pattern for testing one or more of a noise event, a coupling event, a timing event, a race event, and a dynamic hazard.

32. An apparatus for characterizing an electronic circuit comprising:

5   means for receiving circuit design information;

         means for identifying electrical circuit conditions that require test;

         means for selecting a first design verification test;

         means for evaluating the effectiveness of the first design verification test in exercising the identified electrical circuit condition; and

10   means for selecting a second design verification test when the first design verification test is found to be ineffective.